TABLE I. DEVICE

PARAMETERS 1/

JPL PART # ST12214-	MFG.	GENERIC PART #	PACKAGE STYLE	DETAIL SCREENING TESTS	ELECTRICAL CHARACTERISTICS & GROUP A TESTS	RADIATION (TID) LEVEL RAD(Si)
QM7130MR	INR	IRHM7130	TO-254 2/	Table III	Table IV	100k 3/

NOTES:

1/ This drawing, in conjunction with CS515581, imposes all requirements for procurement of these devices.

2/ Device physical dimensions shall conform to MIL-S-19500, Appendix F, Figure 21.

Lead designation shall be: Terminal number 1 - Drain
Terminal number 2 - Source
Terminal number 3 - Gate

3/ Steady state total dose irradiation tests shall be conducted per MIL-S-19500, Group D, Subgroup 2 and Table V herein.

4. This standard takes precedence over documents referenced herein.

TABLE II. MANUFACTURERS MAXIMUM RATINGS (T_C=25°C)

PARAMETER	RATING	UNITS
V_{DS}/V_{DG}	100	Vdc
V_{GS}	±20	Vdc
I_D	14	Adc
I_{DM}	56	A_{pk}
$R_{\theta(J-C)}$	1.67	°C/W
T_J, T_{STG}	-55 TO 150	°C

RELEASED THRU SECTION 356 DATA MANAGEMENT: DATE:

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APPROVED SOURCE(S)

THE ITEM LISTED IN THE APPROVED SOURCE BLOCK AND IDENTIFIED BY VENDOR NAME, ADDRESS, AND PART NUMBER WILL BE EVALUATED AND TESTED BY THE JPL ELECTRONIC PARTS RELIABILITY SECTION OR ITS DELEGATED ALTERNATE BEFORE BEING APPROVED FOR USE. NON-JPL USERS SHALL CHECK WITH THE ELECTRONIC PARTS RELIABILITY SECTION ON THE STATUS OF THE PART'S APPROVAL BEFORE USING.

VENDOR PART NO	VENDOR	JPL PART NO

JET PROPULSION LABORATORY CALIFORNIA INSTITUTE OF TECHNOLOGY

CAGE NO 23835

Procurement specification: CS515581
Screening specification: ZPP-2073-GEN

TITLE: TRANSISTOR, POWER MOSFET N CHANNEL, RAD HARD

DETAIL SPECIFICATION

ST 12214

Custodian: Electronic Parts Reliability Section 514

SHEET 1 OF 4

FILE (Sec. 514): F:\USERS\514\SPECS\ACT-DETL\ST12214.A

TABLE III. DETAIL SCREENING REQUIREMENTS

SCREEN (SEE MIL-S-19500, TABLE II)	TEST CONDITIONS/REQUIREMENTS
3c. THERMAL RESPONSE 1/	MIL-STD-750, METHOD 3161.
9. INTERIM ELECTRICAL PARAMETERS	I_{GSSF1}, I_{GSSR1}, I_{DSS1} (TEST CONDITIONS AND LIMITS OF TABLE IV)
10. HIGH TEMPERATURE REVERSE BIAS (HTRB)	MIL-STD-750, METHOD 1042, CONDITION B.
11. INTERIM ELECTRICAL AND DELTA PARAMETERS	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(ON)1}$, $V_{GS(th)1}$ (TEST CONDITIONS AND LIMITS OF TABLE IV). DELTA LIMITS: ΔI_{GSSF1} = ±20 nA OR ±100% OF INITIAL VALUE, WHICHER IS GREATER. ΔI_{GSSR1} = ±20 nA OR ±100% OF INITIAL VALUE, WHICHER IS GREATER. ΔI_{DSS1} = ±10 uA OR ±100% OF INITIAL VALUE, WHICHEVER IS GREATER. Δr_{DSON1} = ±20% OF INITIAL VALUE. $\Delta V_{GS(th)1}$ = ±20% OF INITIAL VALUE.
12. BURN-IN	MIL-STD-750, METHOD 1042, CONDITION A
13. FINAL ELECTRICAL TESTS A. PARAMETERS B. DELTA LIMITS	 SUBGROUPS 2 AND 3 OF TABLE IV HEREIN SAME PARAMETERS AND LIMITS AS 11 ABOVE.

1/ Shall be performed any time before screen 10.

TABLE IV. GROUP A ELECTRICAL TESTS

TEST	MIL-STD-750 METHOD	TEST CONDITIONS	LIMITS		
			MIN	MAX	UNITS
SUBGROUP 2 (T_C=25°C) DRAIN-SOURCE BREAKDOWN VOLTAGE, B_{VDSS}	3407	I_D = 1mA, V_{GS} = 0	100		Vdc
GATE CURRENT, I_{GSSF1}	3411	V_{GS} = +20 Vdc, V_{DS} = 0		100	nA
GATE CURRENT, I_{GSSR1}	3411	V_{GS} = -20 Vdc, V_{DS} = 0		100	nA
DRAIN CURRENT, I_{DSS1}	3413	V_{DS} = 80 Vdc, V_{GS} = 0		25	uA
GATE TO SOURCE THRESHOLD VOLTAGE, $V_{GS(th)}$	3403	$V_{DS} \geq V_{DS}$, I_D = 1 mA	2	4	Vdc
DRAIN-SOURCE ON RESISTANCE, $R_{DS(ON)1}$	3421	V_{GS} = 12 Vdc, I_D = 5 A 1/		.18	Ω
DRAIN-SOURCE ON RESISTANCE, $R_{DS(ON)2}$	3421	V_{GS} = 12 Vdc, I_D = 8 A 1/		.20	Ω
FORWARD VOLTAGE, V_{SD}	4011	I_S = 8 A, V_{GS} = 0 1/		1.8	Vdc
SUBGROUP 3 (T_C=125°C) GATE CURRENT, I_{GSSF2}	3411	V_{GS} = +20 Vdc, V_{DS} = 0		200	nA
GATE CURRENT, I_{GSSR2}	3411	V_{GS} = -20 Vdc, V_{DS} = 0		200	nA
DRAIN CURRENT, I_{DSS2}	3413	V_{DS} = 80 Vdc, V_{GS} = 0		250	uA
GATE TO SOURCE THRESHOLD VOLTAGE, $V_{GS(th)2}$	3403	$V_{DS} \geq V_{GS}$, I_D = 1 mA	1		Vdc
DRAIN-SOURCE ON RESISTANCE, $R_{DS(ON)3}$	3421	V_{GS} = 12 Vdc, I_D = 5 A 1/		.35	Ω
LOW TEMP OPERATION GATE TO SOURCE THRESHOLD VOLTAGE, $V_{GS(th)3}$	3403	$V_{DS} \geq V_{DS}$, I_D = 1 mA T_C = -55°C		5	Vdc
SUBGROUPS 4 THROUGH 7 2/					

NOTES:

1/ PULSE TEST: Pulse width ≤ 300usec; Duty Cycle ≤ 2%.

2/ These tests not applicable unless specified.

TABLE V. TID TESTS AND POST IRRADIATION PARAMETRIC LIMITS

TEST 1/ 2/	MIL-STD-750 METHOD	TEST CONDITIONS	LIMITS (POST IRRADIATION)		
			MIN	MAX	UNITS
SUBGROUP 2 T_c=25°C STEADY-STATE TOTAL DOSE IRRADIATION, (V_{GS} BIAS) 3/	1019	V_{GS}= 12 Vdc V_{DS}= 0			
STEADY-STATE TOTAL DOSE IRRADIATION, (V_{DS} BIAS) 3/	1019	V_{GS}= 0 V_{DS}= 80 Vdc			
END POINT ELECTRICALS DRAIN-SOURCE BREAKDOWN VOLTAGE, BV_{DSS}	3407	I_D= 1 mA	100		Vdc
GATE TO SOURCE VOLTAGE THRESHOLD, $V_{GS(th)}$	3404	$V_{DS} \geq V_{GS}$ I_D= 1.0 mA	2	4	Vdc
GATE CURRENT, I_{GSS}	3411	V_{GS}= 20 Vdc V_{DS}= 0		100	nA
GATE CURRENT, I_{GSS}	3411	V_{GS}= -20 Vdc, V_{DS}= 0		-100	nA
DRAIN CURRENT, I_{DSS}	3413	V_{DS}= 80 Vdc, V_{GS}= 0		50	uA
DRAIN-SOURCE ON RESISTANCE, $R_{DS(ON)}$	3421	V_{GS}= 12 Vdc, I_D= 5 A 4/		.18	Ω

NOTES:

1/ For sampling plan, see MIL-S-19500.

2/ Irradiation tests may be performed anytime prior to lot formation. Wafers meeting the TID requirements may be used for any other detail specification utilizing the same die design.

3/ Seperate samples shall be used for each bias.

4/ PULSE TEST: Pulse width ≤ 300usec; Duty Cycle ≤ 2%.

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