DEVICE PARAMETERS 1/, 3/

JPL PART NO.	MANUFACTURER	GENERIC PART NO.	RADIATION LEVEL (TID) (RADS) 2/	PACKAGE STYLE	TERMINAL CONNECTIONS	ELECTRICAL PERFORMANCE CHARACTERISTICS	ELECTRICAL TEST REQUIREMENTS	BURN-IN CONNECTION TABLE
12154 - E01060FR	HONEYWELL SSEC	HR1060 - DCC	100K	FIG. 5-3 HEREIN (84-LEAD FLATPACK)	FIG. 5-1 HEREIN	TABLE 4-4 & 4-5 HEREIN	TABLE 4-1 HEREIN	TABLE 4-7 HEREIN

NOTES: 1/ THIS DRAWING, IN CONJUNCTION WITH CS515837B AND MIL-I-38535, LEVEL Q, IMPOSES ALL REQUIREMENTS FOR PROCUREMENT OF THESE DEVICES.
2/ THE POST-IRRADIATION PARAMETRIC LIMITS SHALL BE THOSE OF TABLES 4-4 & 4-5 HEREIN.
3/ THIS STANDARD TAKES PRECEDENCE OVER DOCUMENTS REFERENCED HEREIN.

RELEASED THRU SECTION 356 DATA MANAGEMENT: DATE:

REVISION: B APPROVED BY (Section 514): DATE:

APPROVED BY (Section 348): DATE:

APPROVED SOURCE(S)

VENDOR PART NO.	VENDOR	JPL PART NO.
22016641	HONEYWELL INC. SOLID STATE ELECTRONIC CENTER PLYMOUTH, MN 55441 CAGE NO. 34168	12154 - E01060FR

The item listed in the approved source block and identified by vendor name, address, and part number will be evaluated and tested by the JPL Electronic Parts Reliability Section or its delegated alternate before being approved for use. Non-JPL users shall check with the Electronic Parts Reliability Section on the status of the part's approval before using.

JET PROPULSION LABORATORY CALIFORNIA INSTITUTE OF TECHNOLOGY CAGE NO. 23835

Procurement Specification: CS515837

Screening Specification: CS515837, ST12154

Custodian: Parts Reliability Group Section 514

TITLE:

MICROCIRCUIT, DIGITAL, ASIC, GATE ARRAY, DATA COMPRESSION CHIP (DCC)

DETAILED SPECIFICATION

ST 12154

SHEET 1 OF 28

FILE: (Sec.514): F:\USERS\514\SPECS\ACT-DETL\ST12154.B

CHANGE INCORPORATION LOG

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Scope

This is the detailed specification for a space-qualified Data Compression Chip (DCC) Application Specific Integrated Circuit (ASIC) gate array for the Cassini Imaging Science Subsystem. This document shall be the sole source of design specifications for the DCC gate array, and shall supersede any other specification documents issued prior to this release.

Applicable Documents

- *General Specification for Gate Array Application Specific Integrated Circuits (ASICs), 24 March 1992, CS515837, Rev. B*

  This document establishes the general design system, manufacturing and testing requirements for the gate array Application Specific Integrated Circuit (ASIC) parts.

- *ISFLIP Compression Chip (ICC) Algorithm Definition, JPL D-6914, December 1989.*

  This document describes the noiseless coding algorithms used for the ISFLIP Compression Chip (ICC) and details the output format for the compressed data.

1. CHIP OVERVIEW

1.1 Data Compression Chip Features

- Lossless data compression chip capable of 2:1 average compression ratio
- Implemented in a Honeywell HR1060 Radiation Hardened CMOS Gate Array
- Screened to QML Level Q
- User-selectable internal or external prediction
- Input data samples can be 8 through 12-bits wide
- 16-bit output data bus to send compressed data
- Built-in-test capabilities
- Operates at 5 MHz clock rate (minimum) under worst case process, temperature, voltage and radiation conditions
- Single +5V Power Supply

1.2 Description

The algorithmic definition for the Cassini Data Compression Chip is identical to that for the HIRIS Data Compression Chip, which is described in JPL D-6914. However, there are significant differences between the two devices, as generic features have been added to the Cassini Data Compression Chip to make it applicable to the data compression problems of a larger class of instruments and subsystems. The added features are:

1) The input data samples can be 8, 9, 10, 11 or 12-bits wide, and the desired sample width is user selectable. For the HIRIS Data Compression Chip, the width of input data samples is fixed at 12-bits.

2) The sample predictions can be internal (previous sample) or external (an external source supplies each prediction as an input to the chip); the desired prediction method is user selectable. (A user may select external prediction if, for example, it is determined that frame-to-frame correlation of a data set will provide a higher compression ratio than sample-to-sample correlation.) In the HIRIS Data Compression Chip, internal prediction must be used since no alternative prediction method was provided.

The functional block diagram for the Cassini Data Compression Chip is shown in Figure 1-1.

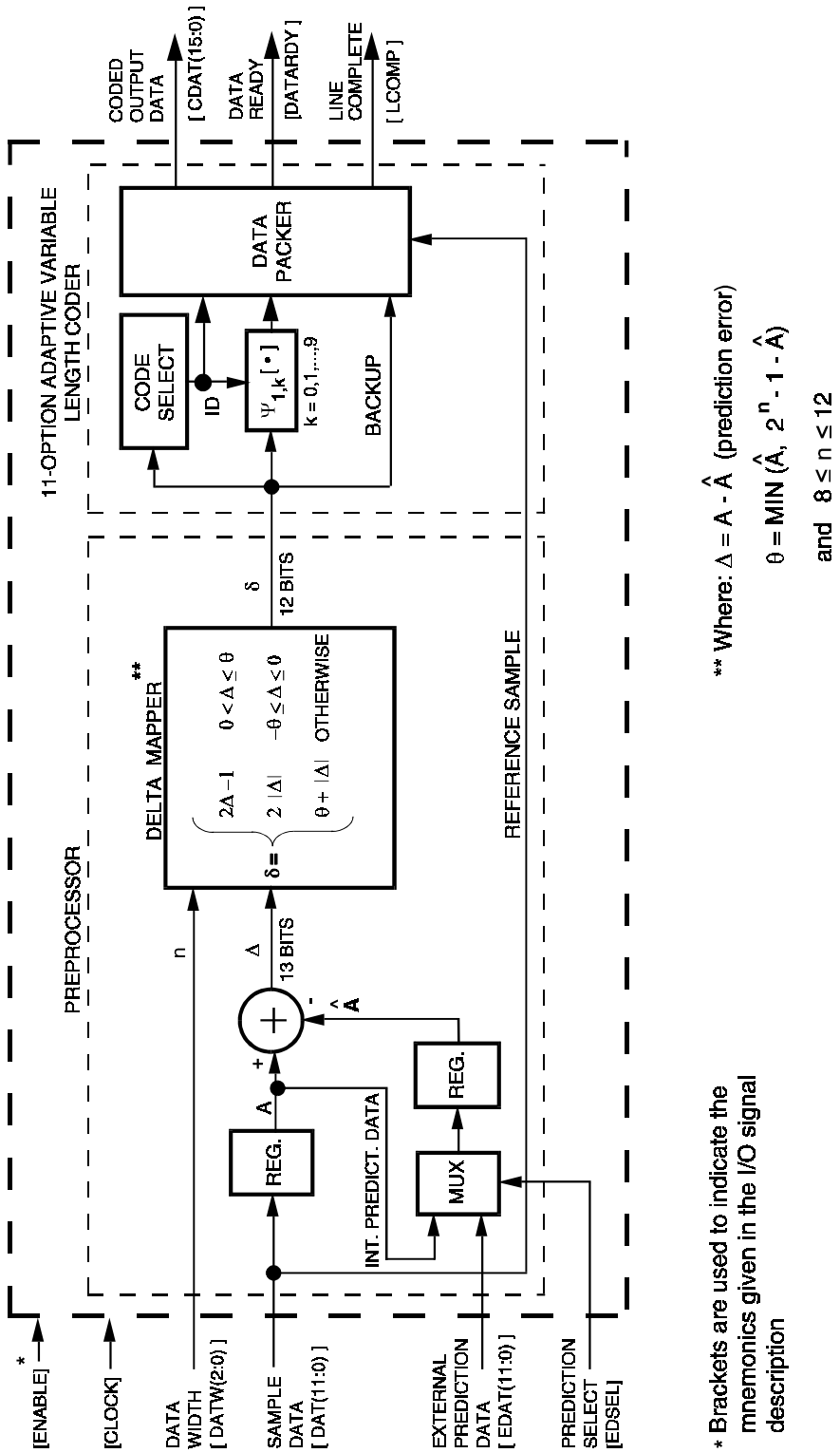


Figure 1-1. DCC Block Diagram

2. FUNCTIONAL DESCRIPTION

2.1 Sampling of Input Data

The compressor will begin processing input data from the DAT(11:0) bus after ENABLE goes high on the next rising edge of CLOCK. Sample 1 is the data on DAT(11:0) after ENABLE makes its low to high transition.
The timing diagram in Figure 2-1 illustrates this sequence.

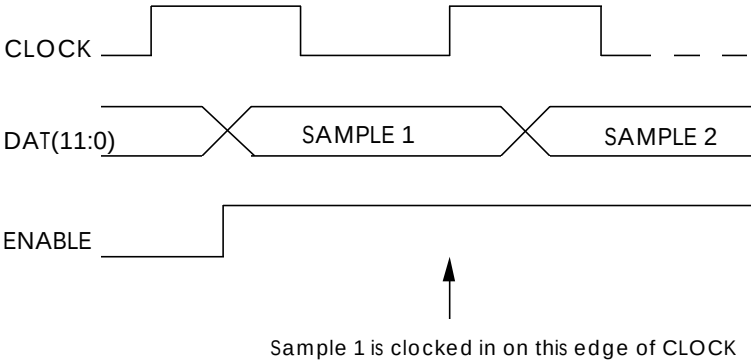


Figure 2-1. Sampling of Input Data (Sample 1)

Minimum setup and hold times from: (a) DAT(11:0) to the rising edge of CLOCK and (b) ENABLE high/low to the rising edge of CLOCK must be met. Subsequent samples on DAT(11:0) are clocked in on the rising edge of CLOCK while ENABLE is high. The last sample of the variable length line is defined as the data on DAT(11:0) at the last rising edge of CLOCK before ENABLE makes its high to low transition, as illustrated in the diagram in Figure 2-2.

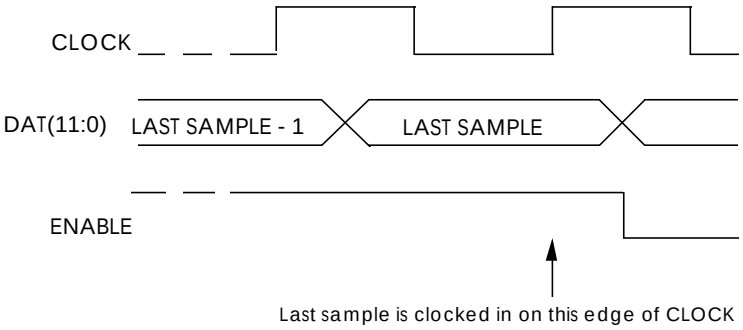


Figure 2-2. Sampling of Input Data (Last Sample)

<u>Application Note:</u>

After the falling edge of ENABLE, the compressor chip is not immediately ready to receive another line of input data. A minimum of 67 clocks is required between the falling edge of ENABLE and the next rising edge of ENABLE to be certain that the compressor has done the following:

(1) flushed out the compressed data from the previous line, and
(2) reinitialized its control logic to be ready to receive a new line of input data.

There is an alternative to counting 67 clocks between ENABLEs. Following the falling edge of ENABLE, the LCOMP output signal can be monitored while the compressor chip is clocked with ENABLE=0. The assertion of LCOMP signifies that all of the compressed data has been output from the previous line. After LCOMP is generated, the compressor chip must either receive at least 16 additional clocks with ENABLE held in the low logic state, or it must be reset. The chip will then be set up to receive a new line of input data.

2.2 Sampling of Input Data when External Prediction is Selected

If External Prediction is selected, then EDSEL must be set high prior to the start of a line of samples (i.e. prior to the rising edge of ENABLE). This is illustrated in the diagram in Figure 2-3.

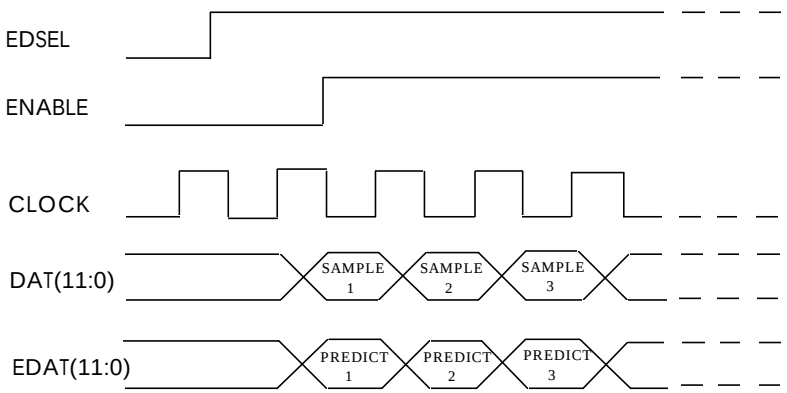


Figure 2-3. Sampling of Input Data (External Prediction)

While External Prediction is selected, both DAT(11:0) and the corresponding value for EDAT(11:0) must be input to the chip on the same rising edge of CLOCK.

2.3 Validation of Compressed Output Data

The coded output data from the compression chip is accessed from the 16-bit compressed data output bus, CDAT(15:0). The data on the bus is valid when it is stable and when the Data Ready signal, DATARDY, is high. The diagram in Figure 2-4 illustrates this.

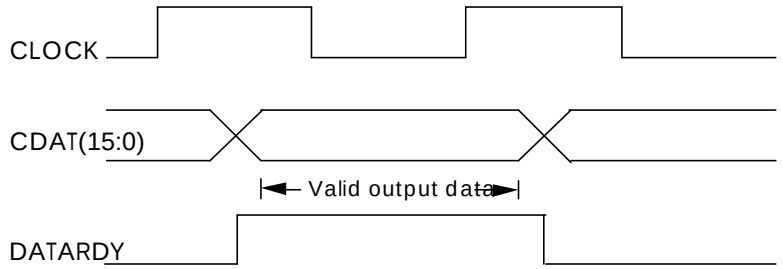


Figure 2-4. Validation of Compressed Output Data

While DATARDY is high, each 16-bit group of data in the output data string should be accessed on the rising edge of CLOCK. While DATARDY is low, the data on CDAT(15:0) should be ignored.

2.4 Observation of Test Output Data

On the third rising edge of CLOCK after ENABLE makes its low to high transition, valid data will be present on the TDAT(15:0) bus. On every subsequent rising edge of CLOCK while ENABLE remains high, the data on TDAT(15:0) will be valid. These timing relationships are shown in the diagram in Figure 2-5.

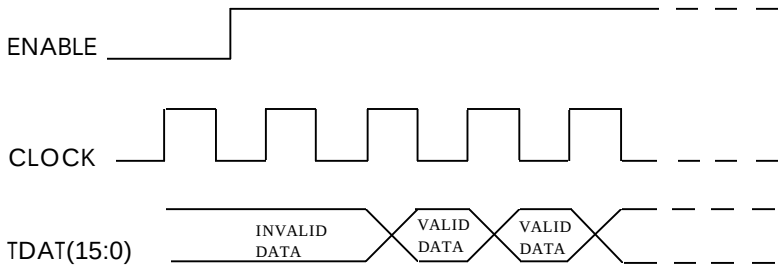


Figure 2-5. Observation of Test Output Data

As explained in the I/O signal description, the data fields that are output on TDAT(15:0) are controlled by TESTDS.

2.5 Summary of Key Operational Restrictions and Requirements

1) The nRESET signal must be held in the low logic state for a minimum of 2 complete clock periods after the chip is powered-up. It must be held in the high logic state before the first rising edge of ENABLE.

2) The input sample data width is selected by controlling the DATW(2:0) bus. If a data width of less than 12-bits is selected, then the appropriate number of MSBs of DAT(11:0) must be held in the low logic state.

3) The DATW(2:0) bus may be changed before the start of a line of input samples. The minimum setup time of DATW(2:0) before the rising edge of ENABLE must be met. A data width that has been selected for a line of input samples must remain constant for the entire line.

4) If external prediction is selected and any of the MSBs of DAT(11:0) are being held in the low logic state for the selection of a data width of less than 12-bits, then the corresponding MSBs of EDAT(11:0) must also be held in the low logic state.

5) After the falling edge of ENABLE, the compressor chip is not immediately ready to receive another line of input data. A minimum of 67 clocks is required between the falling edge of ENABLE and the next rising edge of ENABLE to be certain that the compressor has done the following :

   (1) flushed out the compressed data from the previous line, and
   (2) reinitialized its control logic to be ready to receive a new line of input data.

   (There is an alternative to counting 67 clocks between ENABLEs. Following the falling edge of ENABLE, the LCOMP output signal can be monitored while the compressor chip is clocked with ENABLE=0. The assertion of LCOMP signifies that all of the compressed data has been output from the previous line. After

LCOMP is generated, the compressor chip must either receive at least 16 additional clocks with ENABLE held in the low logic state, or it must be reset. The chip will then be set up to receive a new line of input data.)

6) A line of input data must contain a minimum of 32 samples. There is no limit on the maximum number of samples in a line.

7) For operational use, SELTEST must be held in the low logic state, as this input is only used during test to force the selection of an externally specified code option.

3. DCC ASIC SIGNAL DESIGNATIONS AND DESCRIPTIONS

3.1 I/O Signal Description

All I/O signals are CMOS voltage-compatible with the exception of both input data buses, DAT(11:0) and EDAT(11:0), which are TTL voltage-compatible.

3.1.1 Inputs

DAT(11:0) 12-bit bus for receiving input sample data. The input samples can be 8 through 12-bits wide. The user selects the data width by controlling the DATW(2:0) bus and by forcing the appropriate number of MSBs of DAT(11:0) to logical zero:

	DATW(2)	DATW(1)	DATW(0)	
8-bit data	0	0	0	and force D(11)=D(10)=D(9)=D(8) = 0
9-bit data	0	0	1	and force D(11)=D(10)=D(9) = 0
10-bit data	0	1	0	and force D(11)=D(10) = 0
11-bit data	0	1	1	and force D(11) = 0
12-bit data	1	X	X	where X = don't care

EDAT(11:0) 12-bit bus for receiving external prediction data. The data on EDAT(11:0) is clocked into the compressor on the rising edge of CLOCK while EDSEL = 1. The data on EDAT(11:0) is ignored while EDSEL = 0. (Note: If EDSEL = 1 and any of the MSBs of DAT(11:0) have been forced to zero for the selection of a data width of less than 12-bits, then the corresponding MSBs of EDAT(11:0) *must* also be forced to zero).

EDSEL Select line for external prediction data. When EDSEL = 1, external prediction is selected, and the predictions are received on the EDAT(11:0) bus. When EDSEL = 0 internal prediction is selected, and the predicted value is the previous input sample (previous value of DAT(11:0)). (Note: If EDSEL = 1 and all the bits of EDAT(11:0) = 0, the compressor's preprocessor will be effectively bypassed, because under these conditions the mapped differences that are output from the DELTA MAPPER module will be equal to the input samples themselves. This feature would be used either for test purposes or when preprocessing of input samples is done externally).

ENABLE Enable data line. The processing of input samples is enabled while this signal is asserted (ENABLE=1) and is disabled while this signal is quiescent (ENABLE=0).

CLOCK Input samples will be clocked into the compressor on the rising edge of CLOCK while ENABLE=1. Compressed output data shall be accessed from the compressor on the rising edge of CLOCK while DATARDY=1.

nRESET Active low reset signal to the compressor's controller and output modules. The nRESET signal must be held low for a minimum of 2 complete clock periods after the chip is powered-up. After this is accomplished, the nRESET signal must then be held in the high logic state to allow the compressor to operate. Following the assertion and subsequent de-assertion of nRESET, the compressor is ready to receive the first line of input samples. It is only necessary to assert nRESET

once following chip power-up. While the power remains on, it is not necessary to assert nRESET between consecutive lines of input samples.

TESTDS — Test Data Select Line, used for test purposes only. It controls what information is output on the TDAT(15:0) bus. When TESTDS=0, the 4-bit code ID from the logic of the CODE SELECT module is output on the 4 MSBs and δ from the DELTA MAPPER module is output on the 12 LSBs. When TESTDS=1, the value of the CODE SELECT module's δ summer is output on the TDAT(15:0) bus.

TSTID(3:0) — 4-bit bus to CODE SELECT module, used for test purposes only. When SELTEST=1, the code ID that is output from the CODE SELECT module, CODE(3:0), will take on the value specified by TSTID(3:0).

SELTEST — Test Code ID Select Line. This line is asserted for test purposes only. When SELTEST=1, the CODE(3:0) output bus from the CODE SELECT module is defined by TSTID(3:0). When SELTEST=0, the 4-bit code ID determined by the CODE SELECT module will define CODE(3:0).

DATW(2:0) — Data width control lines. To select 8, 9, 10, 11, or 12-bit data from DAT(11:0). The following table indicates what DATW(2:0) must be to select the desired data width:[1,2]

	DATW(2)	DATW(1)	DATW(0)	
8-bit data	0	0	0	
9-bit data	0	0	1	
10-bit data	0	1	0	
11-bit data	0	1	1	
12-bit data	1	X	X	where X = don't care

3.1.2 Outputs

CDAT(15:0) — 16-bit compressed data output bus.

DATARDY — Data Ready Signal. When asserted (DATARDY=1), this signal indicates the data on CDAT(15:0) is valid for sampling on the rising edge of CLOCK. When DATARDY is quiescent (=0), the data on CDAT(15:0) is not valid.

TDAT(15:0) — 16-bit output bus from the CODE SELECT module, these lines are test outputs. The information that is output on this bus is controlled by TESTDS. When TESTDS=0, the 4-bit code ID from the select logic is output on the 4 MSBs and the output from the DELTA MAPPER module, δ, is output on the 12 LSBs. When TESTDS=1, the value of the CODE SELECT module's δ summer is the output.

---

1 If a data width of less than 12-bits is selected, then the appropriate number of MSBs of DAT(11:0) must be forced to logical zero. (For example, if 8-bit data is selected, then the 4 MSBs of DAT(11:0) must be assigned values of logical zero).

2 A data width that has been selected for a line of input samples must remain constant for the entire line.

LCOMP Line Complete status signal. When asserted (LCOMP=1), this signal indicates that the last word of compressed data has been output on the CDAT(15:0) bus. Thus, LCOMP signifies when the compression of a line of data has been completed. After the falling edge of ENABLE, the compressor chip must receive a minimum of 36 and a maximum of 51 clocks (while ENABLE=0) for the LCOMP signal to be generated. LCOMP is a pulse, one clock period wide, generated on the rising edge of CLOCK. **Following the assertion of LCOMP, the compressor chip must either be reset or it must receive at least 16 additional clocks with the ENABLE signal held in the quiescent state (ENABLE=0).** Either option will cause all of the registers in the controller module to be reinitialized, and then the compressor chip will be ready to accept a new line of input data.

LOADID A control signal generated within the controller module. This signal is a pulse, one clock period wide, generated once per block of input samples on the rising edge of CLOCK. It occurs when CODE(3:0) is latched into the output register of the CODE SELECT module.

4. ELECTRICAL CHARACTERISTICS

4.1 Electrical Test Requirements

Test	**Subgroups** (Per MIL-STD-883, Method 5005, Table 1)
Initial (Pre Burn-In)	1,7
Interim (Post Static I Burn-In)	1*,7*
Delta Calculations*,**	
Interim (Post Static II Burn-In)	1*,7*
Delta Calculations*,**	
Final (Post Dynamic Burn-In)	1*,2,3,7*,8,9,10,11
Delta Calculations*,**	
Group A	1,2,3,7,8,9,10,11
Group C End Point electrical***	1,2,3,7,8,9,10,11
Delta Calculations**	

Table 4-1. Electrical Test Requirements

* PDA applies to these subgroups

** Deltas shall be calculated relative to the initial electrical parameters. Delta limits of Table 5-9 herein shall apply.

*** Group C Lifetest shall be performed using the dynamic burn-in configuration of Table 5-8 herein.

4.2 Absolute Maximum Ratings[3,4,5]

Symbol	Parameter	Ratings		Units
		Min.	Max.	
V_{DD}	Supply Voltage	-0.5	7.0	V
V_{IN}	Input Voltage Range	GND - 0.5	V_{DD} + 0.5	V
I_{OUT}	DC or max. Output Current		25	mA
P_D	Max. Package Power Dissipation		4	W
T_{ST}	Storage Temperature Range	-65	150	^oC
T_S	Lead Temperature (Soldering, 5s)		270	^oC
T_J	Junction Temperature		175	^oC
Θ_{JC}	Thermal Resistance, Junction to Case		4	$^oC/W$
V_{ESD}	ESD Protection Voltage - Class 2 (MIL-STD-883, Method 3015)	2000		V

Table 4-2. Absolute Maximum Ratings

4.3 Recommended Operating Conditions[5,6]

Symbol	Parameter	Ratings		Units
		Min.	Max.	
V_{DD}	Supply Voltage	4.5	5.5	V
T_C	Case Temperature	-55	125	^oC
f_{max}	Max. Operating Frequency		5	MHz

Table 4-3. Recommended Operating Conditions.

---

3 Stresses above the absolute maximum ratings may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and effect reliability.

4 Values are guaranteed but not tested.

5 $-55^oC \leq T_c \leq 125^oC$ except as noted.

6 Extended operation outside recommended limits may degrade performance and effect reliability.

4.4 DC Characteristics

4.4.1 DC Electrical Performance Characteristics

Parameter	Symbol	Test Condition	Subgroup	Limit		Unit
				Min	Max	
Input Threshold Voltage	V_{IH1} [7]	V_{DD}=5.5V	1,2,3		3.85	V
	V_{IH2} [8]	V_{DD}=5.5V			2.0	V
	V_{IL1} [7]	V_{DD}=4.5V	1,2,3	1.35		V
	V_{IL2} [8]	V_{DD}=4.5V		0.8		V
Input Leakage Current	I_{IH}	V_{DD}=5.5V, V_{IH}=V_{DD}	1,2,3	-10	10	µA
	I_{IL}	V_{DD}=5.5V, V_{IL}=GND	1,2,3	-10	10	µA
Output Voltage	V_{OH}	V_{DD}=4.5V, I_{OH}=-6mA	1,2,3	4.0		V
	V_{OL}	V_{DD}=4.5V, I_{OL}=6mA	1,2,3		0.5	V
Output Current	I_{OH}	V_{DD}=4.5V, V_{OH}=4V	1,2,3		-6	mA
	I_{OL}	V_{DD}=4.5V, V_{OL}=0.5V	1,2,3	6		mA
Standby Supply Current	I_{DDSB}	V_{DD}=5.5V, V_{IN}=V_{DD} or GND, Fc=0 Hz	1,2,3		800	µA
Quiescent Current	I_{DDQ}	V_{DD}=5.5V, V_{IN}=V_{DD} or GND, Fc=0 Hz	1		5	µA
Operating Current	I_{DDOP} [9]	V_{DD}=5.5V, V_{IN}=V_{DD} or GND, Fc=5 MHz	1,2,3		80	mA
Input Capacitance [10]	C_{IN}				15	pF
Output Capacitance [10,11]	C_{OUT}				15	pF

Table 4-4. DC Performance Characteristics

---

7 CMOS Inputs: All Inputs, except: DAT(11:0), EDAT(11:0)
8 TTL Inputs: DAT(11:0), EDAT(11:0)
9 This value is based on the supplied functional test vector set and the ANDO tester loading (85 pF) and may not be applicable to system operation.
10 Guaranteed but not tested.
11 Refers to internal capacitance.

4.4.2 Estimated Power Dissipation

$P_{Total} = P_{Internal} + P_{Outputs} + P_{Quiescent} = 212.7 + 87.3 + 4.4 = 304.4$ mW

$P_{Internal} = {}^{1}/_{2} * f_{CLK} * C_{Lint} * (V_{DD})^2 = 212.7$ mW

Where:

C_{Lint}	=	S * #of Nets * 0.75 pF
S	=	0.5
#of Nets	=	7,500 @ 0.75 pF
f_{CLK}	=	5 MHz
V_{DD}	=	5.5 V

$P_{Outputs} = {}^{1}/_{2} * f_{CLK} * C_{Lout} * (V_{DD})^2 + P_{Crowbar} = 79.4 + 7.9 = 87.3$ mW

Where:

C_{Lout}	=	S * #of Output Pads * 50 pF
S	=	0.5
#of Output Pads	=	35 @ 50 pF
f_{CLK}	=	5 MHz
V_{DD}	=	5.5 V
$P_{Crowbar}$	=	10% of $P_{Outputs}$

$P_{Quiescent} = V_{DD} * I_{DDSB} = 4.4$ mW

Where:

V_{DD}	=	5.5 V
I_{DDSB}	=	800 µA

4.4.3 IDDQ Testing

Quiescent Current (IDDQ) testing shall be accomplished by using the Stuck-at Fault test vectors (i.e., Functional test vectors), or a subset thereof, as determined by JPL. Measurements shall be taken at every vector, unless otherwise indicated, recorded and compared to the IDDQ limit. The following statistical values shall be provided: Minimum, Maximum, Mean, Standard Deviation. The IDDQ limits shall be established by JPL after characterization of characterization samples fabricated from the same wafer lot as the flight parts.

4.5 AC Characteristics

4.5.1 AC Electrical Performance Characteristics

Parameter	Symbol	Test Condition $V_{IN}=V_{DD}$ or GND	Subgroup	Specification Limit		Tester Limit [12,13]		Unit
				Min	Max	Min	Max	
Functional Tests		V_{DD}=4.5 & 5.5V Fc=5.0 MHz	7,8	pass		pass		
Propagation Delay:		V_{DD}=4.5 & 5.5V Fc=500 kHz	9,10,11					
CLOCK ↑ to CDAT(15:0)	t_{PHL1} t_{PLH1}		9,10,11	5	39	5	34.0 34.9	ns
CLOCK ↑ to DATARDY	t_{PHL2} t_{PLH2}		9,10,11	5	39	5	34.0 34.9	ns
CLOCK ↑ to TDAT(15:0)	t_{PD1} [14]		9,10,11	5	165			ns
CLOCK ↑ to LCOMP	t_{PHL3} t_{PLH3}		9,10,11	5	39	5	34.0 34.9	ns
CLOCK ↑ to LOADID	t_{PD2} [14]		9,10,11	5	40			ns
Setup Times		V_{DD}=4.5 & 5.5V Fc=500 kHz	9,10,11					
DAT(11:0) to CLOCK ↑	t_{SU1}		9,10,11	12			12	ns
ENABLE to CLOCK ↑	t_{SU2}		9,10,11	8			8	ns
DATW(2:0) to ENABLE ↑	t_{SU3} [14]		9,10,11	136				ns
EDSEL to ENABLE ↑	t_{SU4} [14]		9,10,11	72				ns
EDAT(11:0) to CLOCK ↑	t_{SU5}		9,10,11	6.2			6.2	ns
Hold Times		V_{DD}=4.5 & 5.5V Fc=500 kHz	9,10,11					
CLOCK ↑ to DAT(11:0)	t_{HD1}		9,10,11	28.2			28.2	ns
CLOCK ↑ to ENABLE	t_{HD2}		9,10,11	18			18	ns
CLOCK ↑ to EDAT(11:0)	t_{HD3}		9,10,11	16			16	ns
Min. Pulse Width		V_{DD}=4.5 & 5.5V Fc=500 kHz	9,10,11					
CLOCK high	CPWH		9,10,11	70			70	ns
CLOCK low	CPWL		9,10,11	70			70	ns

Table 4-5. AC Performance Characteristics

[12] Tester limits are shown from a test perspective (i.e., setup time, hold time and min. pulse width are shown as max. limits).
[13] Tester Limits do not include guardbanding for tester errors.
[14] Guaranteed but not tested.

4.5.2 Timing Analysis.

Pre-layout and post-layout timing shall pass the QuickSim simulation of the vectors supplied to the contractor without setup/hold timing violations.

4.5.2.1 Pre-Layout Timing Margins.

Pre-layout timing margins shall be calculated by using standard extreme-value analysis. The extreme values for the cell library shall be supplied by the contractor. Critical paths will be identified and margin calculated via Mentor or Honeywell software toolsets, or a combination thereof.

4.5.2.2 Post-Layout Timing Margins.

Post-layout analysis of the device shall show positive margin on internal critical paths over all operating conditions. The analysis will follow the same form as the pre-layout analysis, with the post-layout timing values annotated to the design file by the contractor.

4.5.2.3 Tester Specification Limits.

Tester Specification limits (max. propagation delays) in Table 4-5 have been adjusted for modified output levels and for differences in output loading in the ANDO tester environment. Modified output levels are required to account for impedance mismatches between device outputs and the ANDO tester environment. For the Ando tester, the output levels for 3 mA buffers are now 1V for low to high transitions and VDD-0.5V for high to low transitions (instead of 50% of VDD). The output levels for the higher drive buffers (6mA, 9mA, 12mA, 15mA) are 1V for low to high transitions and VDD-1V for high to low transitions.

$t_{SPEC}(\text{Tester}) = t_{SPEC}(\text{System}) - (T_{Offset_fixed} + \text{CLoad} * \text{LoadingFactor})$

Where:

C_{Load} = 50 pF (System Load)

For 6 mA drive buffer:

Low to High transition:	T_{Offset_fixed} = -1.0 ns	LoadingFactor = 0.103
High to Low transition:	T_{Offset_fixed} = -1.0 ns	LoadingFactor = 0.121

4.5.5 Tester Load Circuit

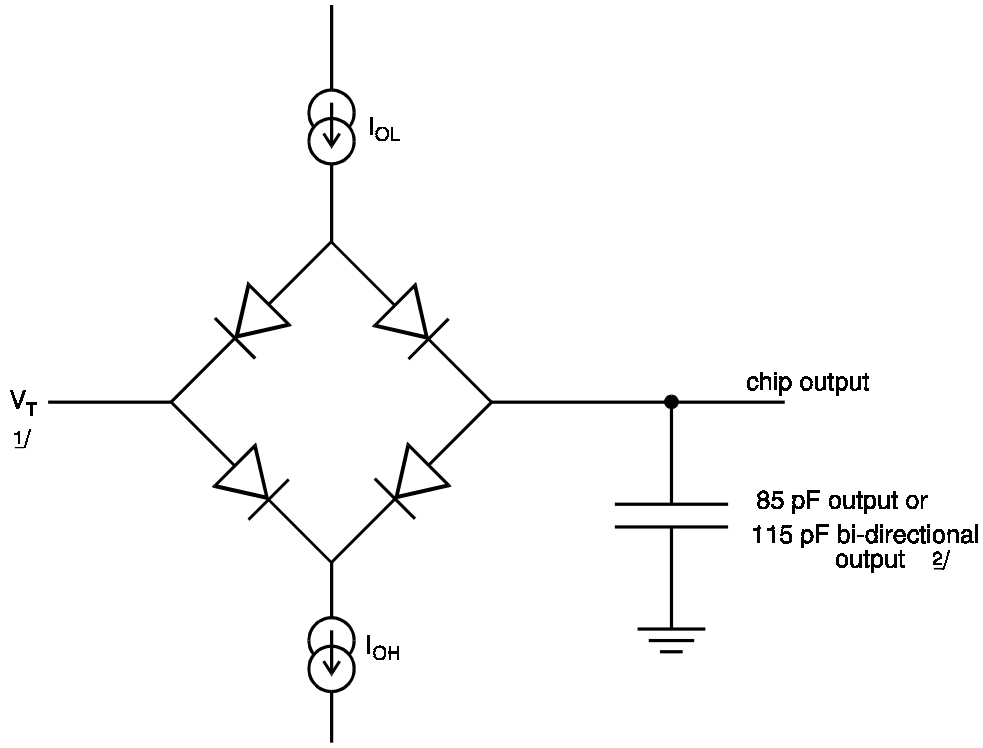


Figure 4-1. Tester Load Circuit

1/ V_T is a variable dependent upon the test parameter.
2/ This capacitance is actually partially distributed through the fixturing and represents the actual loading by a transmission line.

4.6 Burn-In

4.6.1 Static Burn-In

The Static Burn-In conditions shall be as specified in JPL General Specification CS 515837, Rev. B. The burn-in configuration shall be as shown in Table 4-7.

4.6.2 Dynamic Burn-In

The Dynamic Burn-In conditions shall be as specified in JPL General Specification CS 515837, Rev. B. The burn-in configuration shall be as shown in Table 4-7. Input stimuli (STIM) to exercise the device shall be applied by using the functional test vectors, or a subset thereof, plus independently developed test vectors, as determined by JPL. At least one output (MON) shall be monitored during burn-in to assure that the output is toggling and the circuit functioning.

4.6.3 Burn-In Conditions

	Static I	**Static II**	**Dynamic**	**QCI - Life Test**
Duration	48 hours	48 hours	240 hours	2000 hours
Voltage	6.5 V	6.5 V	6.5 V	6.0 V
+ Tolerance	+0.1V	+0.1V	+0.1V *	+0.1V *
- Tolerance	-0.25V	-0.25V	-0.25V	-0.25V
Temperature	125 ^{o}C	125 ^{o}C	125 ^{o}C	125 ^{o}C
+ Tolerance	+5 ^{o}C	+5 ^{o}C	+5 ^{o}C	+5 ^{o}C
- Tolerance	-0 ^{o}C	-0 ^{o}C	-0 ^{o}C	-0 ^{o}C

Table 4-6. Burn-In Conditions

* Applies to Average Power Supply Voltage. Tolerance for Dynamic Switching Noise is +0.25V.

4.6.4 Burn-In Configuration

Signal Name	Pin No.[15]	Type[16]	Burn-In Test Connection[17]			Description
			Static I	Static II	Dynamic	
DAT(11:0)	82 - 84, 1 - 9	TIN	GND	VDD	STIM[18]	Input Sample Data
EDAT(11:0)	73 - 62	TIN	GND	VDD	STIM[18]	External Prediction Data
EDSEL	78	IN	GND	VDD	STIM[18]	Select Line for external Prediction Data
ENABLE	77	IN	GND	VDD	STIM[18]	Enable Data Line
CLOCK	13	IN	GND	VDD	STIM[18]	System Clock
nRESET	76	IN	GND	VDD	STIM[18]	Reset Signal
TESTDS	10	IN	GND	VDD	STIM[18]	Test Data Select Line
TSTID(3:0)	60 - 57	IN	GND	VDD	STIM[18]	Test Input to CODE SELECT Module
SELTEST	61	IN	GND	VDD	STIM[18]	Test Code ID Select Line
DATW(2:0)	81 - 79	IN	GND	VDD	STIM[18]	Data Width Control Lines
CDAT(15:0)	52 - 47, 44 - 40, 38 - 34	OUT6	GND	VDD	VDD[19]	Data Output
DATARDY	45	OUT6	GND	VDD	VDD	Data Ready Signal
TDAT(15:0)	15 - 22, 24 -31	OUT6	GND	VDD	VDD	Test Output from CODE SELECT Module
LCOMP	56	OUT6	GND	VDD	VDD	Line Complete Status Signal
LOADID	55	OUT6	GND	VDD	VDD	Control Signal
VDD	11, 33, 53, 75	VDD	6.5V	6.5V	6.5V (6V for Lifetest)	VDD Power
VSS	12, 14, 23, 32, 39, 46, 54, 74	VSS	0.0V	0.0V	0.0V	VSS Ground

Table 4-7. Burn-In Configuration

[15] The pin numbers of bus signals are in the same sequence as the signals.
[16] For a description of the signal type refer to Table 4-9.
[17] All inputs and outputs shall be tied to the specified voltage level through a 2.2 kΩ resistor (±5%, 1/4W).
[18] Stimulated Inputs
[19] CDAT(0) shall be monitored during burn-in.

4.6.5 Delta Limits

Symbol	Parameter	Spec. Limits		Units	Delta Limits	Units
		Min	Max			
I_{DDSB}	Static Supply Current		800	uA	80	uA
I_{IL}	Input Leakage Current	-10	10	uA	±1	uA
I_{IH}	Input Leakage Current	-10	10	uA	±1	uA
I_{OL}	Output Current		6	mA	±600	uA
I_{OH}	Output Current	-6		mA	±600	uA

Table 4-8. Delta Limits

4.7 Pin Type Description

Pin Name		Drive	I/O	Type
IN	=		CMOS,	Input Signal
TIN	=		TTL,	Input Signal
OUT6	=	6mA,	CMOS,	Output Signal

Table 4-9. Pin Type Description

5. PHYSICAL CHARACTERISTICS

5.1 Pin Assignment

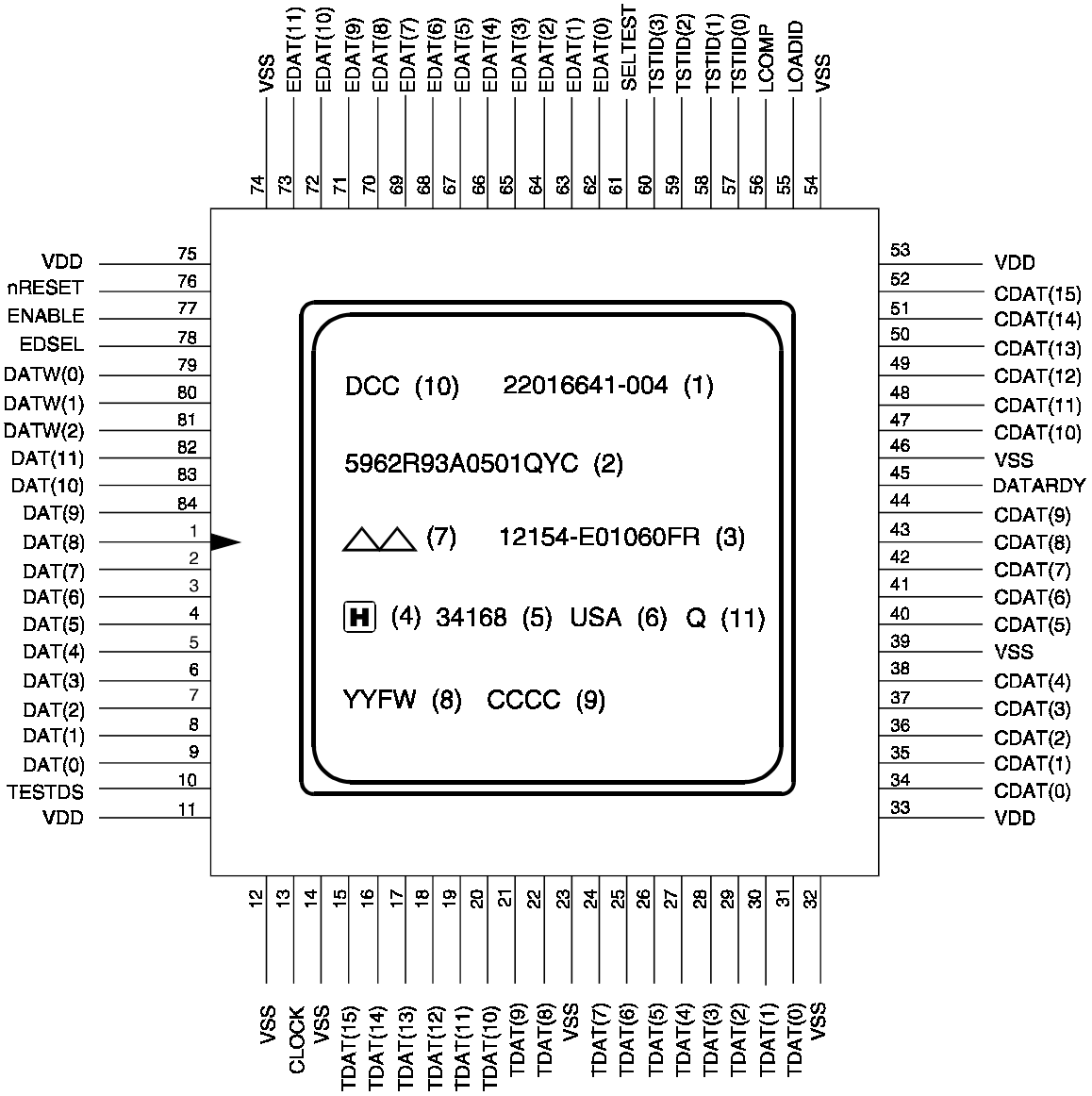


Figure 5-1. DCC Pinout Assignments

5.2 Bonding Diagram

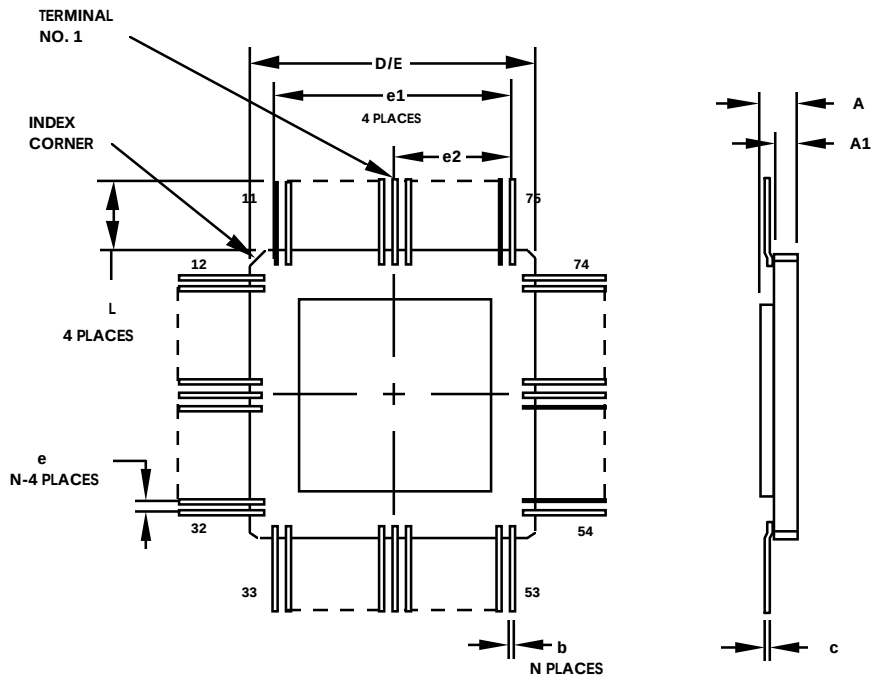
Die Cavity: 520 mil/side
VDD Plane: pins 11, 33, 53, 75
VSS Plane: pins 12, 32, 54, 74
Die Attach: VSS
Lid and Seal Ring: VSS

Figure 5-2. Bonding Diagram (84 pin Flatpack)

5.3 Package Outline

The design shall be compatible with package styles approved by JPL for flight parts, i.e., hermetically sealed ceramic flatpacks, with strain-relieving lead bends.

84 Lead Flat Package



PACKAGE DIMENSIONS		
Symbol	Dimensions in inches	
	min	max
A	0.095	0.125
A1	-	0.105
b	0.014	0.018
c	0.006	0.008
D/E	1.135	1.165
e	0.050 BSC	
e1	1.000 BSC	
e2	0.500 BSC	
L	0.350	-
N	84	

Figure 5-3. Package Outline (84 pin Flatpack)

5.4 Marking Diagram

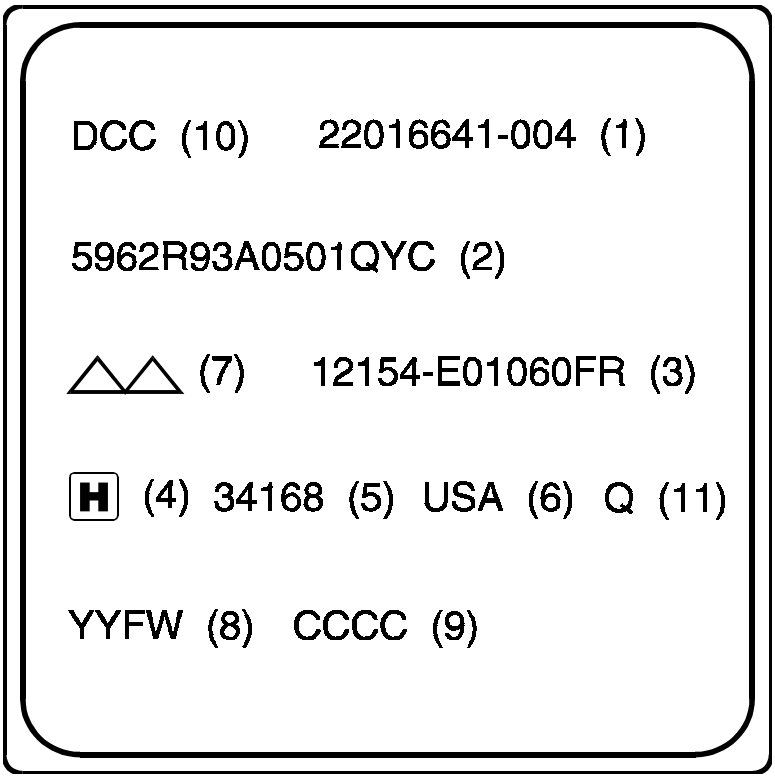


Figure 5-4. Marking Diagram

(1) Honeywell Part Number
(2) QML Number (Flight Units only)
(3) Customer Part Number
(4) Honeywell Trademark
(5) Federal Supplier Manufacturing Number
(6) Country of Origin
(7) Pin 1 indicator and ESD identifier
(8) Date Code -Year and Fiscal Week of Lid Seal.
YY = Year
FW = Fiscal Week
(9) Serialization (Traceability Capability to Die)
(10) Chip Name (If required)
(11) QML Mark (Flight Units only)

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